

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Phase Control Disc Thyristor Type DT80-1250-44

High power cycling capability / Low on-state and switching losses
Designed for traction and industrial applications

Mean on-state current	I_{TAV}		1250 A	
Repetitive peak off-state voltage	V_{DRM}		3800 ÷ 4400 V	
Repetitive peak reverse voltage	V_{RRM}			
Turn-off time	t_q		630, 800 μ s	
V_{DRM}, V_{RRM}, V	3800	4000	4200	4400
Voltage code	38	40	42	44
$T_{j}, ^\circ C$	-60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions
ON-STATE				
I_{TAV}	Mean on-state current	A	1250 1796	$T_c=101^\circ C$, Double side cooled $T_c=85^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TRMS}	RMS on-state current	A	1962	$T_c=101^\circ C$, Double side cooled 180° half-sine wave; 50 Hz
I_{TSM}	Surge on-state current	kA	37.0 43.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			39.0 45.0	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$A^2s \cdot 10^3$	6800 9200	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=10$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			6300 8400	$T_j=T_{jmax}$ $T_j=25^\circ C$ 180° half-sine wave; $t_p=8.3$ ms; single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3800 ÷ 4400	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3900 ÷ 4500	$T_{jmin} < T_j < T_{jmax}$; 180° half-sine wave; single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j=T_{jmax}$; Gate open

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TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j = T_{j\max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j = T_{j\max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	1250	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; $I_{TM} = 7000$ A; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60÷50	
T_j	Operating junction temperature	$^{\circ}$ C	-60÷125	
MECHANICAL				
F	Mounting force	kN	40.0÷50.0	
a	Acceleration	m/s ²	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.10	$T_j = 25$ $^{\circ}$ C; $I_{TM} = 3925$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.164	$T_j = T_{j\max}$;	
r_T	On-state slope resistance, max	m Ω	0.331	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50$ μ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25$ $^{\circ}$ C; $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM} , I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j = T_{j\max}$; $V_D = V_{DRM}$; $V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000, 1600, 2000, 2500	$T_j = T_{j\max}$; $V_D = 0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 150	$T_j = T_{j\min}$ $T_j = 25$ $^{\circ}$ C $T_j = T_{j\max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.40	$T_j = T_{j\max}$;	
I_{GD}	Gate non-trigger direct current, min	mA	45.00	$V_D = 0.67 \cdot V_{DRM}$; Direct gate current	
SWITCHING					
t_{gd}	Delay time, max	μ s	2.75	$T_j = 25$ $^{\circ}$ C; $V_D = 1500$ V; $I_{TM} = I_{TAV}$; $di/dt = 200$ A/ μ s;	
t_{gt}	Turn-on time, max	μ s	12.0	Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50$ μ s; $di_G/dt = 2$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	630, 800	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\max}$; $I_{TM} = I_{TAV}$; $di_R/dt = -5$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	
Q_{rr}	Total recovered charge, max	μ C	6080	$T_j = T_{j\max}$; $I_{TM} = 1250$ A;	
t_{rr}	Reverse recovery time, max	μ s	72	$di_R/dt = -5$ A/ μ s;	
I_{rrM}	Peak reverse recovery current, max	A	169	$V_R = 100$ V	

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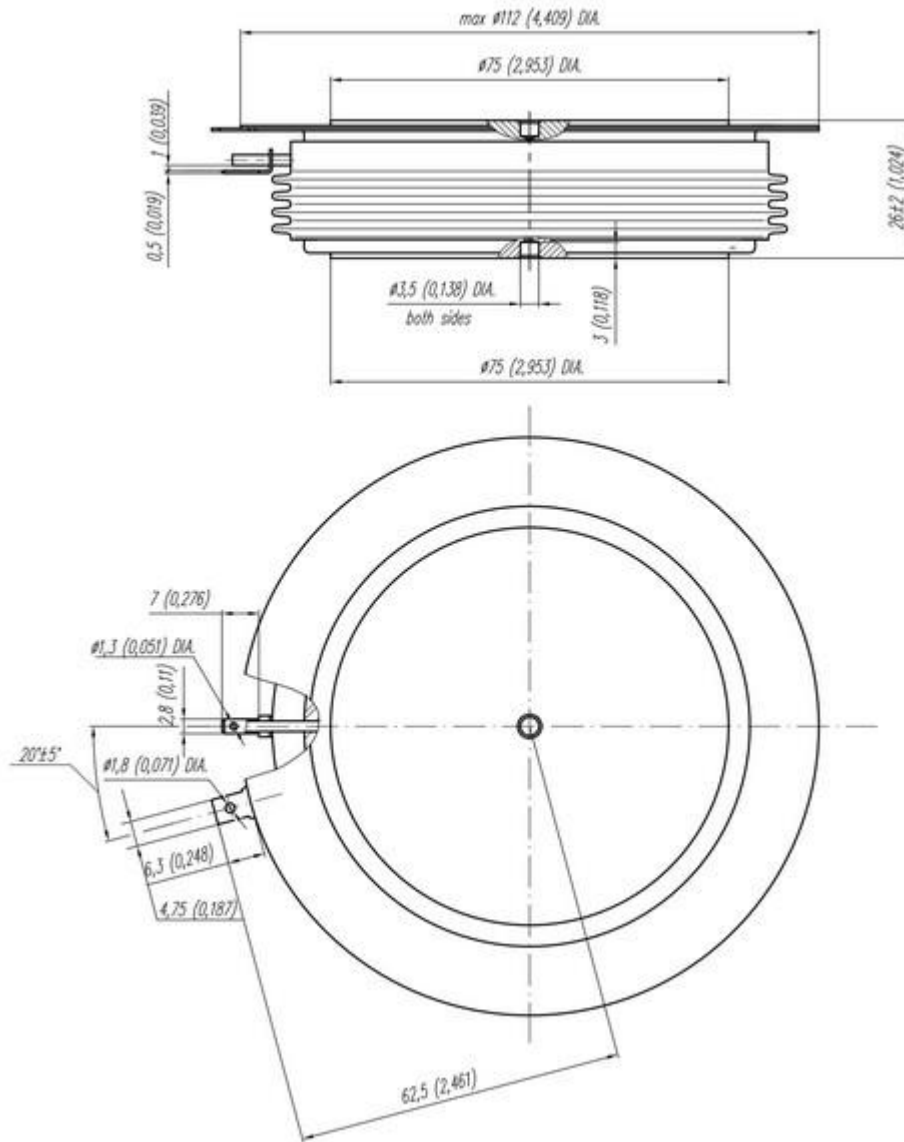
THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0085	Direct current	Double side cooled
R_{thjc-A}			0.0187		Anode side cooled
R_{thjc-K}			0.0153		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0020	Direct current	
MECHANICAL					
w	Weight, max	g	1500		
D_s	Surface creepage distance	mm (inch)	36.60 (1.441)		
D_a	Air strike distance	mm (inch)	16.20 (0.638)		

PART NUMBERING GUIDE							NOTES																							
DT	80	1250	44	7	3		1) Critical rate of rise of off-state voltage <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Symbol of Group</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>8.5</th> <th>9</th> </tr> </thead> <tbody> <tr> <td>$(dv_D/dt)_{crit}, V/\mu s$</td> <td>200</td> <td>320</td> <td>500</td> <td>1000</td> <td>1600</td> <td>2000</td> <td>2500</td> </tr> </tbody> </table>								Symbol of Group	4	5	6	7	8	8.5	9	$(dv_D/dt)_{crit}, V/\mu s$	200	320	500	1000	1600	2000	2500
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1. DT - Phase Control Disc Thyristor 2. Element Diameter 3. Mean on-state current, A 4. Voltage code 5. Critical rate of rise of on-state current non-repetitive, V/ μs 6. Turn-off time ($dv_D/dt=50 V/\mu s$)																														

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OVERALL DIMENSIONS

Package type: T.F2



All dimensions in millimeters (inches)