# EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

# Fast Thyristor Type FDT32-250-30

Low switching losses / Low reverse recovery charge
Distributed amplified gate for high $di_T/dt$

| | | |
|---|---|---|
| Mean on-state current | $I_{TAV}$ | 250 A |
| Repetitive peak off-state voltage | $V_{DRM}$ | 3000 V |
| Repetitive peak reverse voltage | $V_{RRM}$ | |
| Turn-off time | $t_q$ | 50.0; 63.0; 80.0; 100; 125 μs |

| | |
|---|---|
| $V_{DRM}$, $V_{RRM}$, V | 3000 |
| Voltage code | 30 |
| $T_j$, °C | – 60 ÷ 125 |

## MAXIMUM ALLOWABLE RATINGS

| Symbols and parameters | | Units | Values | Test conditions | |
|---|---|---|---|---|---|
| **ON-STATE** | | | | | |
| $I_{TAV}$ | Mean on-state current | A | 250<br>430 | $T_c$= 94 °C; Double side cooled;<br>$T_c$= 55 °C; Double side cooled;<br>180° half-sine wave; 50 Hz | |
| $I_{TRMS}$ | RMS on-state current | A | 390 | $T_c$= 94 °C; Double side cooled;<br>180° half-sine wave; 50 Hz | |
| $I_{TSM}$ | Surge on-state current | kA | 5.7<br>6.6 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 50 Hz ($t_p$=10 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse:$I_G$=$I_{FGM}$; $V_G$=20 V;<br>$t_{GP}$=50 μs; $di_G/dt$=1 A/μs |
| | | | 6.0<br>6.9 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 60 Hz ($t_p$=8.3 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse:$I_G$=$I_{FGM}$; $V_G$=20 V;<br>$t_{GP}$=50 μs; $di_G/dt$=1 A/μs |
| $I^2t$ | Safety factor | $A^2s\cdot10^3$ | 162<br>215 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 50 Hz ($t_p$=10 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse:$I_G$=$I_{FGM}$; $V_G$=20 V;<br>$t_{GP}$=50 μs; $di_G/dt$=1 A/μs |
| | | | 149<br>197 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 60 Hz ($t_p$=8.3 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse:$I_G$=$I_{FGM}$; $V_G$=20 V;<br>$t_{GP}$=50 μs; $di_G/dt$=1 A/μs |
| **BLOCKING** | | | | | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state and Repetitive peak reverse voltages | V | 3000 | $T_{j\,min}$< $T_j$ <$T_{j\,max}$;<br>180° half-sine wave; 50 Hz;<br>Gate open | |
| $V_{DSM}$, $V_{RSM}$ | Non-repetitive peak off-state and Non-repetitive peak reverse voltages | V | 3100 | $T_{j\,min}$< $T_j$ <$T_{j\,max}$;<br>180° half-sine wave; 50 Hz;single pulse;<br>Gate open | |
| $V_D$, $V_R$ | Direct off-state and Direct reverse voltages | V | 0.75·$V_{DRM}$<br>0.75·$V_{RRM}$ | $T_j$=$T_{j\,max}$;<br>Gate open | |

| | | | | |
|---|---|---|---|---|
| **TRIGGERING** | | | | |
| $I_{FGM}$ | Peak forward gate current | A | 6 | $T_j=T_{j\,max}$ |
| $V_{RGM}$ | Peak reverse gate voltage | V | 5 | |
| $P_G$ | Gate power dissipation | W | 3 | $T_j=T_{j\,max}$ for DC gate current |
| **SWITCHING** | | | | |
| $(di_T/dt)_{crit}$ | Critical rate of rise of on-state current non-repetitive (f=1 Hz) | A/μs | 1000 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs; $di_G/dt=1$ A/μs |
| **THERMAL** | | | | |
| $T_{stg}$ | Storage temperature | °C | – 60 ÷ 125 | |
| $T_j$ | Operating junction temperature | °C | – 60 ÷ 125 | |
| **MECHANICAL** | | | | |
| F | Mounting force | kN | 9.0 ÷ 11.0 | |
| a | Acceleration | m/s² | 50<br>100 | Device unclamped<br>Device clamped |

## CHARACTERISTICS

| Symbols and parameters | | Units | Values | Conditions | |
|---|---|---|---|---|---|
| **ON-STATE** | | | | | |
| $V_{TM}$ | Peak on-state voltage, max | V | 3.00 | $T_j=25$ °C; $I_{TM}=785$ A | |
| $V_{T(TO)}$ | On-state threshold voltage, max | V | 1.70 | $T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$ | |
| $r_T$ | On-state slope resistance, max | mΩ | 2.200 | | |
| $I_H$ | Holding current, max | mA | 500 | $T_j=25$ °C; $V_D=12$ V; Gate open | |
| **BLOCKING** | | | | | |
| $I_{DRM}$, $I_{RRM}$ | Repetitive peak off-state and Repetitive peak reverse currents, max | mA | 70 | $T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$ | |
| $(dv_D/dt)_{crit}$ | Critical rate of rise of off-state voltage[1)], min | V/μs | 1000 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open | |
| **TRIGGERING** | | | | | |
| $V_{GT}$ | Gate trigger direct voltage, max | V | 4.00<br>2.50<br>2.00 | $T_j=T_{j\,min}$<br>$T_j=25$ °C<br>$T_j=T_{j\,max}$ | $V_D=12$ V; $I_D=3$ A; Direct gate current |
| $I_{GT}$ | Gate trigger direct current, max | mA | 500<br>300<br>200 | $T_j=T_{j\,min}$<br>$T_j=25$ °C<br>$T_j=T_{j\,max}$ | |
| $V_{GD}$ | Gate non-trigger direct voltage, min | V | 0.25 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current | |
| $I_{GD}$ | Gate non-trigger direct current, min | mA | 10.00 | | |
| **SWITCHING** | | | | | |
| $t_{gd}$ | Delay time | μs | 3.0 | $T_j=25$ °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=50$ μs; $di_G/dt=1$ A/μs | |
| $t_q$ | Turn-off time[2)], max | μs | 50.0; 63.0; 80.0; 100; 125 | $dv_D/dt=50$ V/μs; | $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67\cdot V_{DRM}$ |
| | | | 63.0; 80.0; 100; 125; 160 | $dv_D/dt=200$ V/μs; | |
| $Q_{rr}$ | Total recovered charge, max | μC | 500 | $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; $di_R/dt=-50$ A/μs; $V_R=100$ V | |
| $t_{rr}$ | Reverse recovery time, typ | μs | 5.0 | | |
| $I_{rrM}$ | Peak reverse recovery current, max | A | 200 | | |

## THERMAL

| | | | | | |
|---|---|---|---|---|---|
| $R_{thjc}$ | Thermal resistance, junction to case, max | °C/W | 0.0400 | Direct current | Double side cooled |
| $R_{thjc-A}$ | | | 0.0880 | | Anode side cooled |
| $R_{thjc-K}$ | | | 0.0720 | | Cathode side cooled |
| $R_{thck}$ | Thermal resistance, case to heatsink, max | °C/W | 0.0060 | Direct current | |
| **MECHANICAL** | | | | | |
| w | Weight, typ | g | 180 | | |
| $D_s$ | Surface creepage distance | mm (inch) | 19.44 (0.765) | | |
| $D_a$ | Air strike distance | mm (inch) | 12.10 (0.476) | | |

## NOTES

1) Critical rate of rise of off-state voltage

| Symbol of group | 7 |
|---|---|
| $(dv_D/dt)_{crit}$, V/μs | 1000 |

2)Turn-off time ($dv_D/dt$=50 V/μs)

| Symbol of group | 2 | 1 | | 4 | |
|---|---|---|---|---|---|
| $t_q$, μs | 50.0 | 63.0 | 80.0 | 100 | 125 |

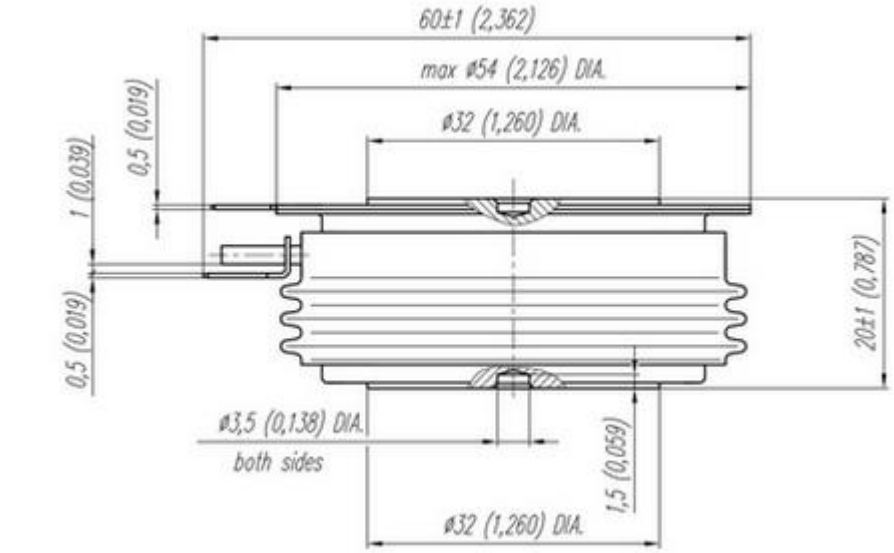
## PART NUMBERING GUIDE

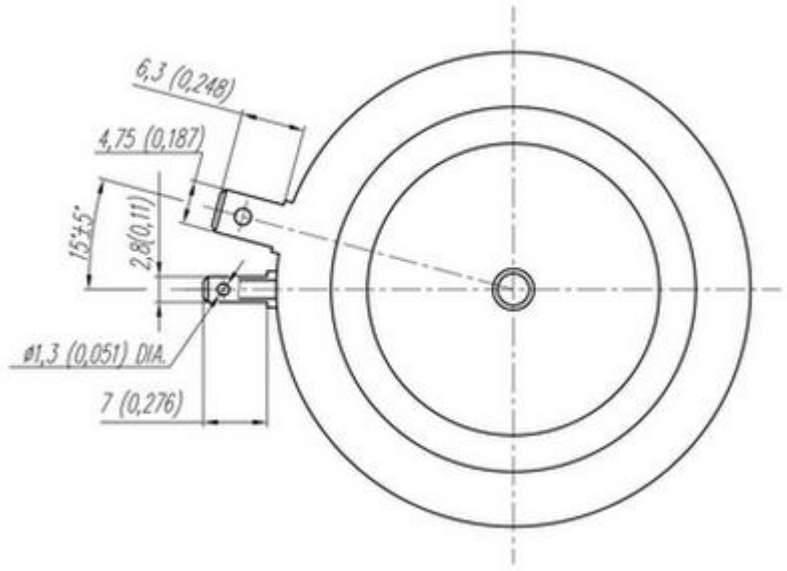
| FDT | 32 | 250 | 30 | 7 | 4 | |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | |

1. FDT — Fast Inverter Disc Thyristor
2. Element Diameter
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time ($dv_D/dt$=50 V/μs)

## OVERALL DIMENSIONS

**Package type: T.B3**




All dimensions in millimeters (inches)



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