

EVLYS LTD. - POWER SEMICONDUCTORS DEVICES -

Wholesale and Retail.

Fast Inverter Thyristor Type FIDT56-1000-14

Low switching losses / Low reverse recovery charge

Distributed amplified gate for high di_T/dt

Mean on-state current		I_{TAV}	1000 A		
Repetitive peak off-state voltage		V_{DRM}	1000...1400 V		
Repetitive peak reverse voltage		V_{RRM}			
Turn-off time		t_q	10.0, 12.5, 16.0, 20.0 μs		
V_{DRM}, V_{RRM}, V	1000	1100	1200	1300	1400
Voltage code	10	11	12	13	14
$T_j, ^\circ C$	$-60...+125$				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	871 1000 1318	$T_c = 85^\circ C$; Double side cooled; $T_c = 77^\circ C$; Double side cooled; $T_c = 55^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	1570	$T_c = 77^\circ C$; Double side cooled; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	23.0 26.0	$T_j = T_{j \max}$ $T_j = 25^\circ C$	180° half-sine wave; $t_p = 10$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
			24.0 28.0	$T_j = T_{j \max}$ $T_j = 25^\circ C$	180° half-sine wave; $t_p = 8.3$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
I^2t	Safety factor	$A^2s \cdot 10^3$	2600 3300	$T_j = T_{j \max}$ $T_j = 25^\circ C$	180° half-sine wave; $t_p = 10$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
			2300 3200	$T_j = T_{j \max}$ $T_j = 25^\circ C$	180° half-sine wave; $t_p = 8.3$ ms; single pulse; $V_D = V_R = 0$ V; Gate pulse: $I_G = I_{FGM}$; $V_G = 20$ V; $t_{GP} = 50$ μs ; $di_G/dt = 1$ A/ μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000...1400	$T_{j \min} < T_j < T_{j \max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100...1500	$T_{j \min} < T_j < T_{j \max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6 \cdot V_{DRM}$ $0.6 \cdot V_{RRM}$	$T_j = T_{j \max}$; Gate open	

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TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j = T_{j \max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	8	$T_j = T_{j \max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive ($f=1$ Hz)	A/ μ s	2500	$T_j = T_{j \max}; V_D = 0.67 \cdot V_{DRM}; I_{TM} = 2200$ A; Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50 \mu$ s; $di_G/dt = 2$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	°C	-60...+50	
T_j	Operating junction temperature	°C	-60...+125	
MECHANICAL				
F	Mounting force	kN	24.0...28.0	
a	Acceleration	m/s ²	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	2.50	$T_j = 25$ °C; $I_{TM} = 3140$ A
$V_{T(TO)}$	On-state threshold voltage, max	V	1.520	$T_j = T_{j \max};$
r_T	On-state slope resistance, max	mΩ	0.312	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$
I_H	Holding current, max	mA	500	$T_j = 25$ °C; $V_D = 12$ V; Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	150	$T_j = T_{j \max};$ $V_D = V_{DRM}; V_R = V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	200, 320, 500, 1000, 1600, 2000, 2500	$T_j = T_{j \max};$ $V_D = 0.67 \cdot V_{DRM};$ Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	$T_j = T_{j \min}$ $T_j = 25$ °C $T_j = T_{j \max}$
I_{GT}	Gate trigger direct current, max	mA	500 300 150	$T_j = T_{j \min}$ $T_j = 25$ °C $T_j = T_{j \max}$
V_{GD}	Gate non-trigger direct voltage, min	V	0.40	$T_j = T_{j \max}; V_D = 0.67 \cdot V_{DRM};$
I_{GD}	Gate non-trigger direct current, min	mA	60.00	Direct gate current
SWITCHING				
t_{gd}	Delay time, max	μ s	0.90	$T_j = 25$ °C; $V_D = 600$ V; $I_{TM} = I_{TAV};$ $di/dt = 200$ A/ μ s;
t_{gt}	Turn-on time ²⁾ , max	μ s	2.00, 2.50, 3.20, 4.00	Gate pulse: $I_G = 2$ A; $V_G = 20$ V; $t_{GP} = 50 \mu$ s; $di_G/dt = 2$ A/ μ s
t_q	Turn-off time ³⁾ , max	μ s	10.0, 12.5, 16.0, 20.0	$T_j = T_{j \max};$ $I_{TM} = I_{TAV};$ $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$
			12.5, 16.0, 20.0, 25.0	$dv_D/dt = 200$ V/ μ s;
Q_{rr}	Total recovered charge, max	μ C	150	$T_j = T_{j \max}; I_{TM} = 1000$ A;
t_{rr}	Reverse recovery time, typ	μ s	4.0	$di_R/dt = -50$ A/ μ s;
I_{rrM}	Peak reverse recovery current, max	A	100	$V_R = 100$ V

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THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	$^{\circ}\text{C}/\text{W}$	0.0210	Direct current	Double side cooled
R_{thjc-A}			0.0462		Anode side cooled
R_{thjc-K}			0.0378		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	$^{\circ}\text{C}/\text{W}$	0.0040	Direct current	

MECHANICAL					
w	Weight, max	g	510		
D_s	Surface creepage distance	mm (inch)	31.60 (1.244)		
D_a	Air strike distance	mm (inch)	16.50 (0.649)		

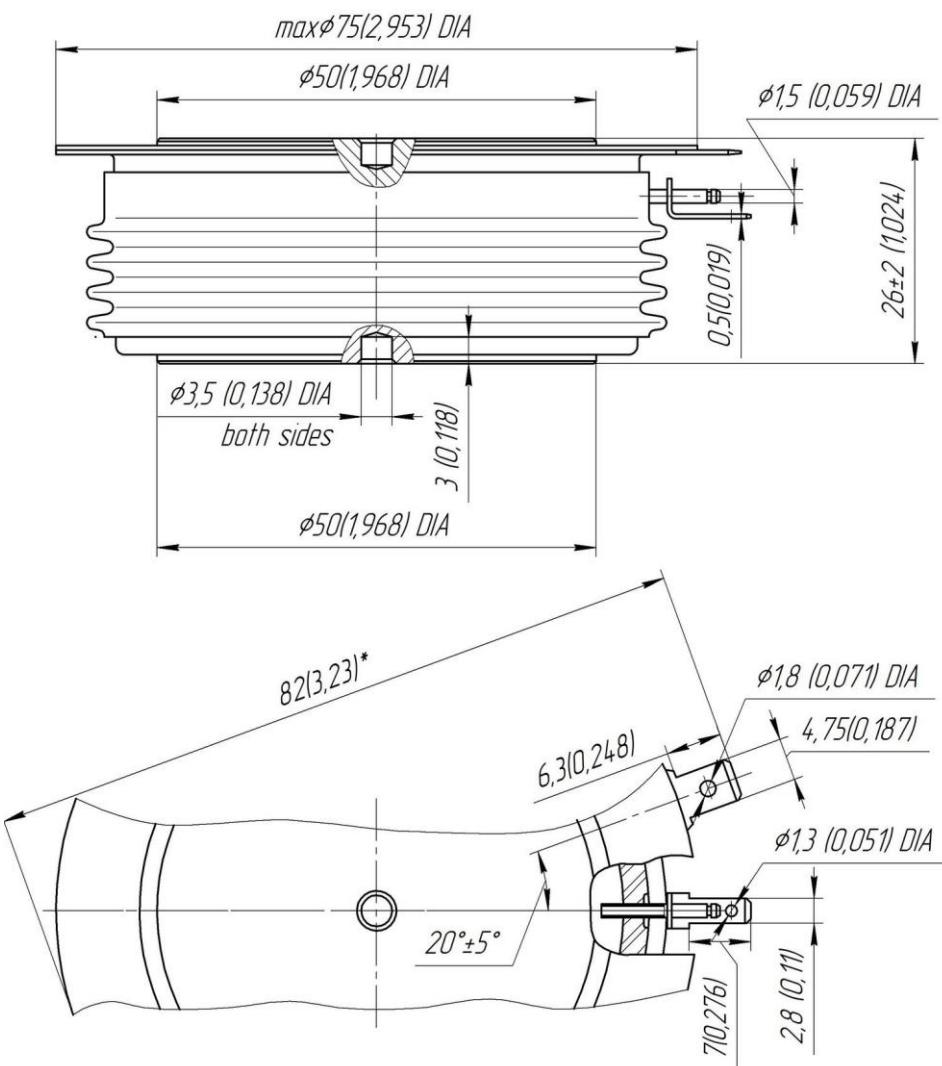
PART NUMBERING GUIDE							NOTES						
FIDT	56	1000	14	7	8	3							
1	2	3	4	5	6	7							
1. FIDT — Fast Inverter Disc Thyristor with Distributed Amplified Gate							1) ¹⁾ Critical rate of rise of off-state voltage						
2. Element Diameter							Symbol of Group	4	5	6	7	8	8,5
3. Mean on-state current, A							$(dv_0/dt)_{crit}, \text{V}/\mu\text{s}$	200	320	500	1000	1600	2000
4. Voltage code													2500
5. Critical rate of rise of off-state voltage							2) ²⁾ Turn-on time						
6. Group of turn-off time ($dv_D/dt=50 \text{ V}/\mu\text{s}$)							Symbol of group	5	4	3	2		
7. Group of turn-on time							$t_{gt}, \mu\text{s}$	2.00	2.50	3.20	4.00		
							3) ³⁾ Turn-off time ($dv_D/dt=50 \text{ V}/\mu\text{s}$)						
							Symbol of group	8	7	6			
							$t_{go}, \mu\text{s}$	10.0	12.5	16.0	20.0		

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OVERALL DIMENSIONS

Package type: T.D5



All dimensions in millimeters (inches)

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