EVLYS LTD. - POWER SEMICONDUCTORS DEVICES - Wholesale and Retail.

Fast Stud Thyristor Type FST32C-250-14

Pressure contact / Low switching losses / Low reverse recovery charge
High power cycling capability / Distributed amplified gate for high di_T/dt

Mean on-state current			I_{TAV}	250 A	
Repetitive peak off-state voltage			V_{DRM}	1000...1400 V	
Repetitive peak reverse voltage			V_{RRM}		
Turn-off time			t_q	25.0, 32.0, 40.0, 50.0 μs	
V_{DRM}, V_{RRM}, V	1000	1100	1200	1300	1400
Voltage code	10	11	12	13	14
T_j, °C	–60...+125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Maximum allowable mean on-state current	A	250 266 399	T_c=88 °C; T_c=85 °C; T_c=55 °C; 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	392	T_c=88 °C; 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	7.0 8.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			7.5 8.5	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
I^2t	Safety factor	$A^2s{\cdot}10^3$	240 320	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
			230 290	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=50 μs; di_G/dt=1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000...1400	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100...1500	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.6·V_{DRM} 0.6·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	1600	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; I_{TM}=500 A; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs
THERMAL				
T_{stg}	Storage temperature	°C	–60...+50	
T_j	Operating junction temperature	°C	–60...+125	
MECHANICAL				
F	Mounting force	kN	1.5...2.5	
a	Acceleration	m/s^2	100	

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.80	T_j=25 °C; I_{TM}=785 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.168	$T_j=T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.915		
I_H	Holding current, max	mA	500	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/µs	200, 320, 500, 1000, 1600, 2000, 2500	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.50 1.50	T_j= $T_{j\,min}$ T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	400 250 150	T_j= $T_{j\,min}$ T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.40	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	35.00		
SWITCHING					
t_{gd}	Delay time, max	µs	0.70	T_j=25 °C; V_D=600 V; $I_{TM}=I_{TAV}$; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs	
t_{gt}	Turn-on time[2)], max	µs	1.60, 2.00, 2.50, 3.20		
t_q	Turn-off time[3)], max	µs	25.0, 32.0, 40.0, 50.0	dv_D/dt=50 V/µs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; di_R/dt=-10 A/µs; V_R=100V; V_D=0.67 V_{DRM}	
Q_{rr}	Recovered charge, max	µC	200	$T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; di_R/dt=-50 A/µs; V_R=100 V	
t_{rr}	Reverse recovery time, max	µs	4.0		
I_{rr}	Reverse recovery current, max	A	100		

THERMAL				
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.085	Direct current
MECHANICAL				
m	Weight, max	g	500	
D_s	Surface creepage distance	mm (inch)	12.4 (4.882)	
D_a	Air strike distance	mm (inch)	12.4 (4.882)	

PART NUMBERING GUIDE

FST	32C	250	14	7	4	5	
1	2	3	4	5	6	7	

1. FST — Fast Inverter Stud Thyristor
2. Design version
3. Mean on-state current, A
4. Voltage code
5. Critical rate of rise of off-state voltage
6. Group of turn-off time (dv_D/dt=50 V/μs)
7. Group of turn-on time

NOTES

1) Critical rate of rise of off-state voltage

Symbol of Group	4	5	6	7	8	8,5	9
$(dv_D/dt)_{crit}$, V/μs	200	320	500	1000	1600	2000	2500

2)Turn-on time

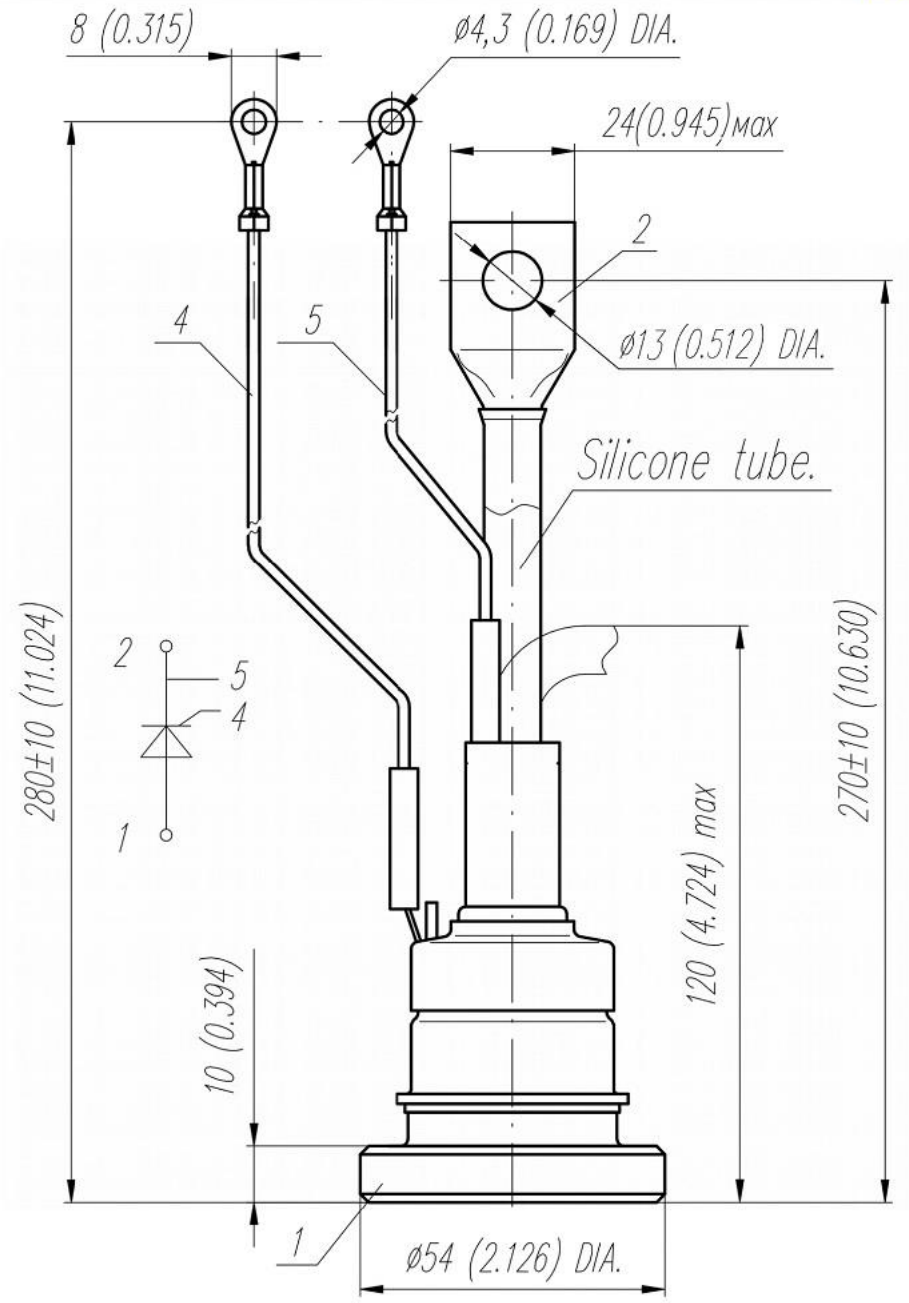
Symbol of group	6	5	4	3
t_{gt}, μs	1.60	2.00	2.50	3.20

3)Turn-off time (dv_D/dt=50 V/μs)

Symbol of group	5	4	3	2
t_q, μs	25.0	32.0	40.0	50.0

OVERALL DIMENSIONS

Package type: T.SB3



Polarity	Example of code designation	Reference designation	Colors		
			Anode	Cathode	Gate
Anode to stud	FST32_75		-	Red tube	White

All dimensions in millimeters (inches)